

4-Line Capacitance TVS Diode Array

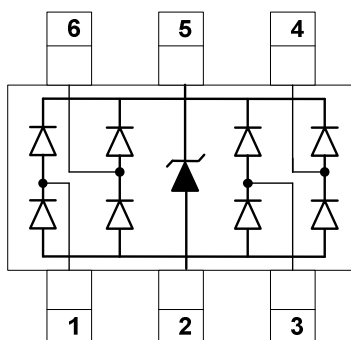
Description

The USRV05-4 is a low capacitance TVS array, utilizing leading monolithic silicon technology to provide fast response time and low ESD clamping voltage, making this device an ideal solution for protecting voltage sensitive high-speed data lines. The USRV05-4 complies with the IEC 61000-4-2 (ESD) standard with $\pm 30\text{kV}$ air and $\pm 25\text{kV}$ contact discharge. It is assembled into a 6-lead SOT23-6 lead-free package. The leads are finished with lead-free matte tin. Each device will protect up to four high-speed lines. The combination of small size, low capacitance, and high surge capability makes them ideal for use in applications such as 10/100 Ethernet, USB 2.0, and video interfaces.

Mechanical Characteristics

- ◆ Package: SOT23-6
- ◆ Lead Finish: Matte Tin
- ◆ UL Flammability Classification Rating 94V-0
- ◆ Case Material: "Green" Molding Compound
- ◆ Moisture Sensitivity: Level 3 per J-STD-020
- ◆ Terminal Connections: See Diagram Below
- ◆ Marking Information: See Below

Dimensions and Pin Configuration



Circuit and Pin Schematic

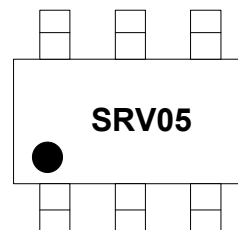
Features

- ◆ Low capacitance: 1.8pF typical (I/O to I/O)
- ◆ Ultra low leakage: nA level
- ◆ Low operating voltage: 5V
- ◆ Low clamping voltage
- ◆ Up to 4 lines and one power line protects
- ◆ Complies with following standards:
 - IEC 61000-4-2 (ESD) immunity test
 - Air discharge: $\pm 30\text{kV}$
 - Contact discharge: $\pm 25\text{kV}$
 - IEC61000-4-4 (EFT) 40A (5/50ns)
 - IEC61000-4-5 (Lightning) : 18A(8/20 μs)
- ◆ ROHS Compliant

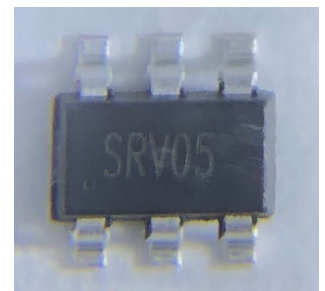
Applications

- ◆ USB 2.0 power and data line
- ◆ Monitors and flat panel displays
- ◆ Set-top box and digital TV
- ◆ Video graphics cards
- ◆ Digital video interface(DVI)
- ◆ Notebook Computers
- ◆ SIM Ports
- ◆ 10/100 Ethernet
- ◆ IEEE 1394 firewire ports

Marking Information



SRV05 = Device Marking Code
Dot denotes Pin1



Ordering Information

Part Number	Marking	Packaging	Reel Size
USRV05-4	SRV05	3000/Tape & Reel	7 inch

Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

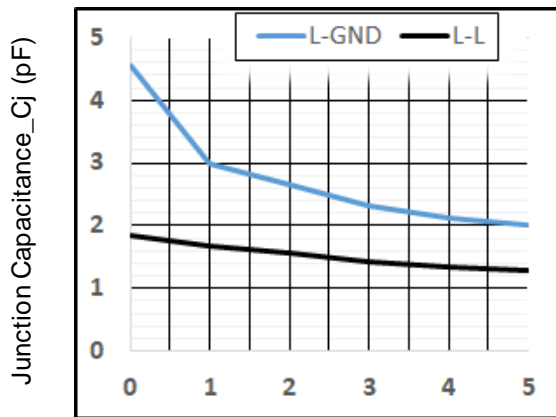
Parameter	Symbol	Value	Unit
Peak Pulse Power (tp=8/20μs)	PPP	450	W
Peak Pulse Current (tp=8/20μs)	I _{PP}	18	A
ESD per IEC 61000-4-2 (Air)	V _{ESD}	±30	kV
ESD per IEC 61000-4-2 (Contact)		±25	
Operating Temperature Range	T _J	-55 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

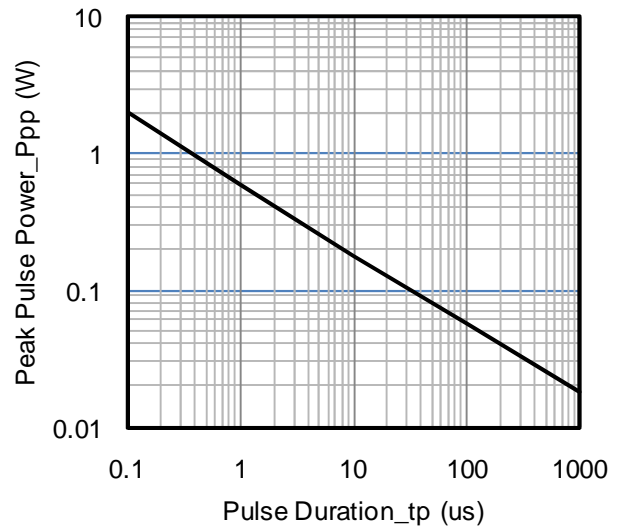
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V _{RWM}			5	V	Pin 5 to Pin 2
Breakdown Voltage	V _{BR}	6			V	I _T = 1mA, Pin 5 to Pin 2
Reverse Leakage Current	I _R			1	μA	V _{RWM} = 5V, Pin 5 to Pin 2
Clamping Voltage	V _C			12	V	I _{PP} = 1A (8 x 20μs pulse) any I/O pin to ground
	V _C			17	V	I _{PP} = 18A (8 x 20μs pulse) any I/O pin to ground
	V _C			12	V	I _{PP} = 1A (8 x 20μs pulse) between I/O pins
	V _C			25	V	I _{PP} = 18A (8 x 20μs pulse) between I/O pins
Forward Voltage	V _F			1.2	V	I _F = 15mA
Junction Capacitance	C _J		1.8		pF	V _R = 0V, f = 1MHz, between I/O pins
Junction Capacitance	C _J			5.0	pF	V _R = 0V, f = 1MHz, any I/O pin to ground

Note 1: I/O pins are Pin 1, 3, 4 and 6

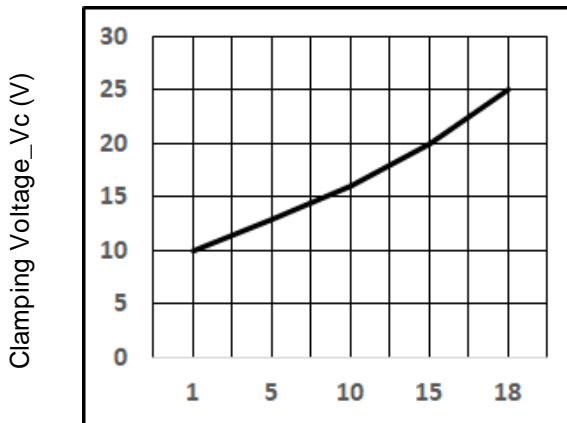
Typical Performance Characteristics (TA=25°C unless otherwise Specified)



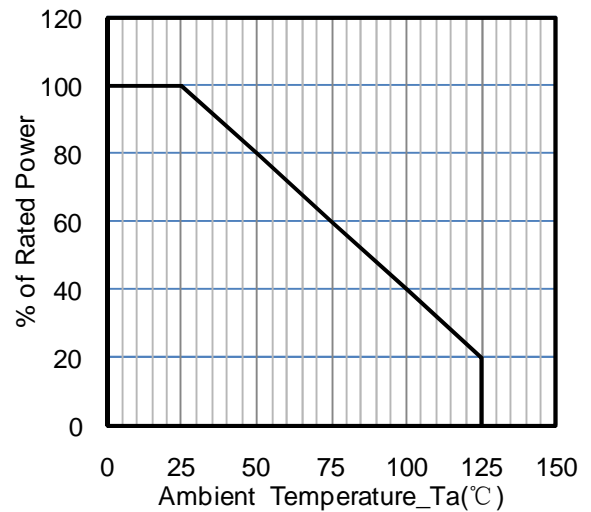
Reverse Voltage_VR (V)
Junction Capacitance vs. Reverse Voltage



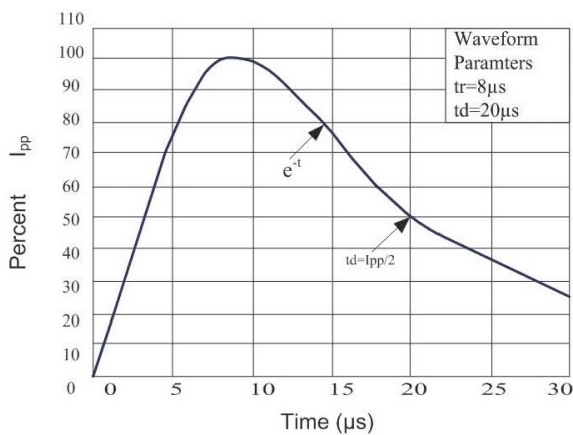
Pulse Duration_tp (us)
Peak Pulse Power vs. Pulse Time



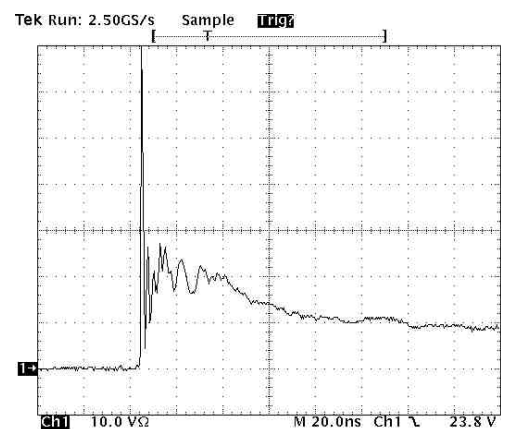
Peak Pulse Current_Ipp (A)
Clamping Voltage vs. Peak Pulse Current



Power Derating Curve



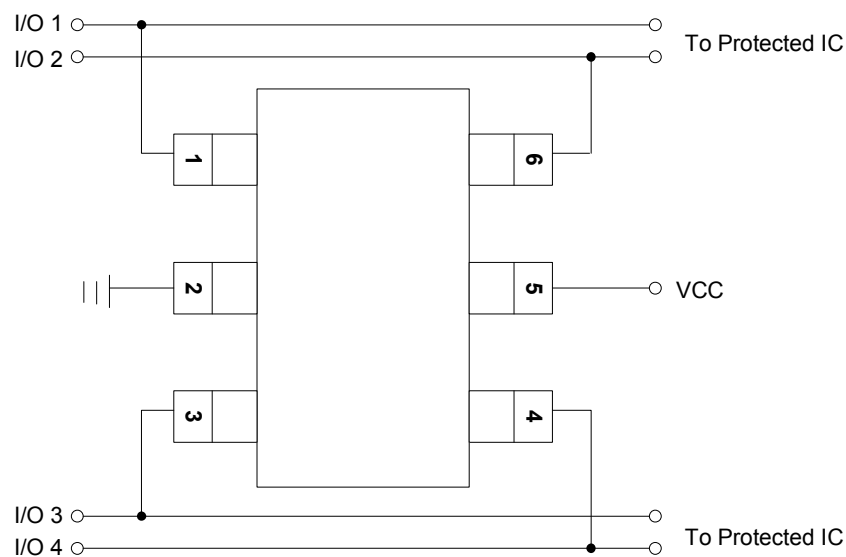
8 X 20uS Pulse Waveform



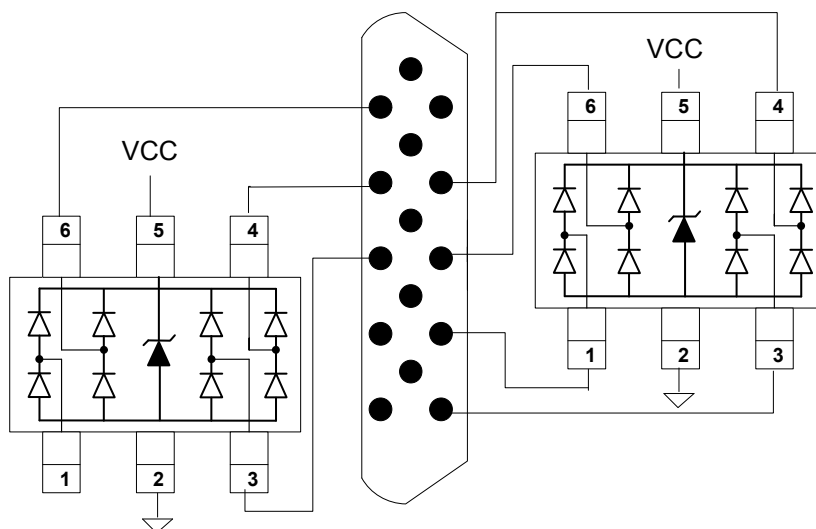
ESD Clamping Voltage
8 kV Contact per IEC61000-4-2

Typical Application

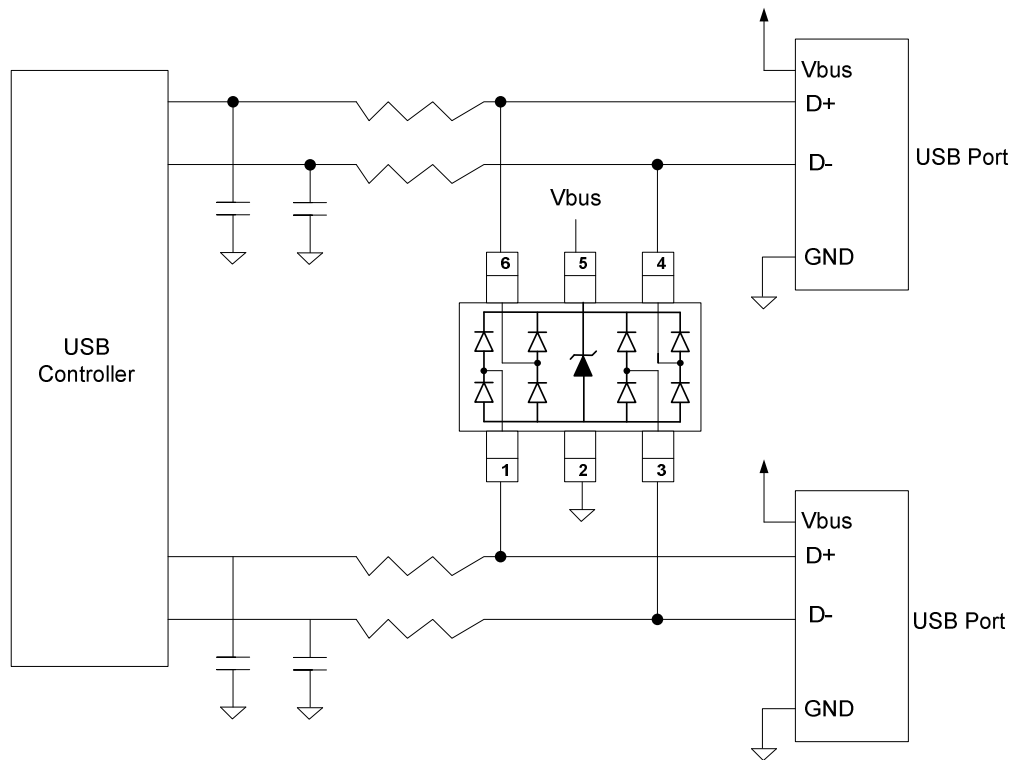
The USRV05-4 is designed to protect four data lines from transient over-voltages by clamping them to fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode VF) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. The negative reference (REF1) is connected at pin 2. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference (REF2) is connected at pin 5.



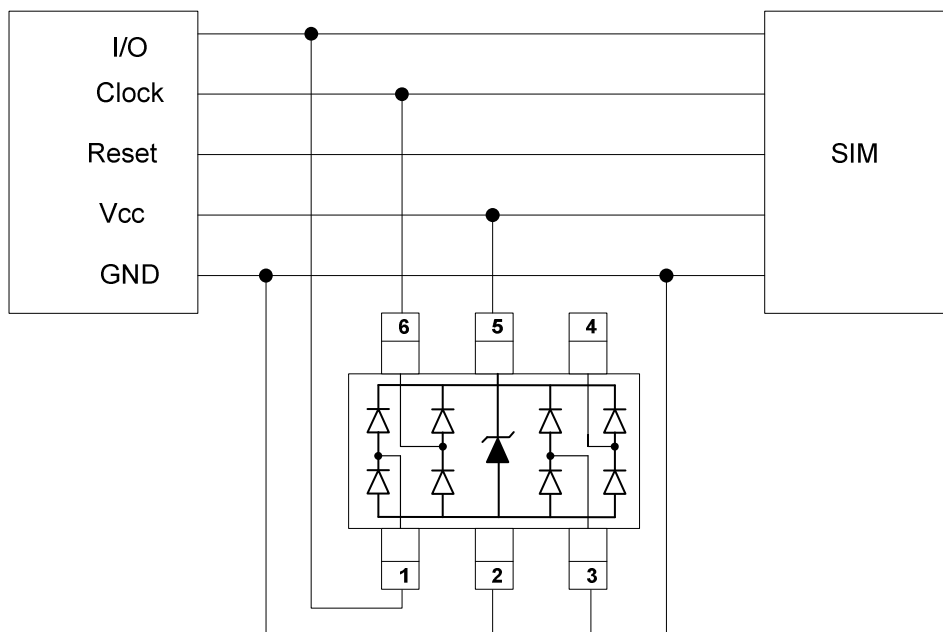
USRV05-4 on Video Interface Application



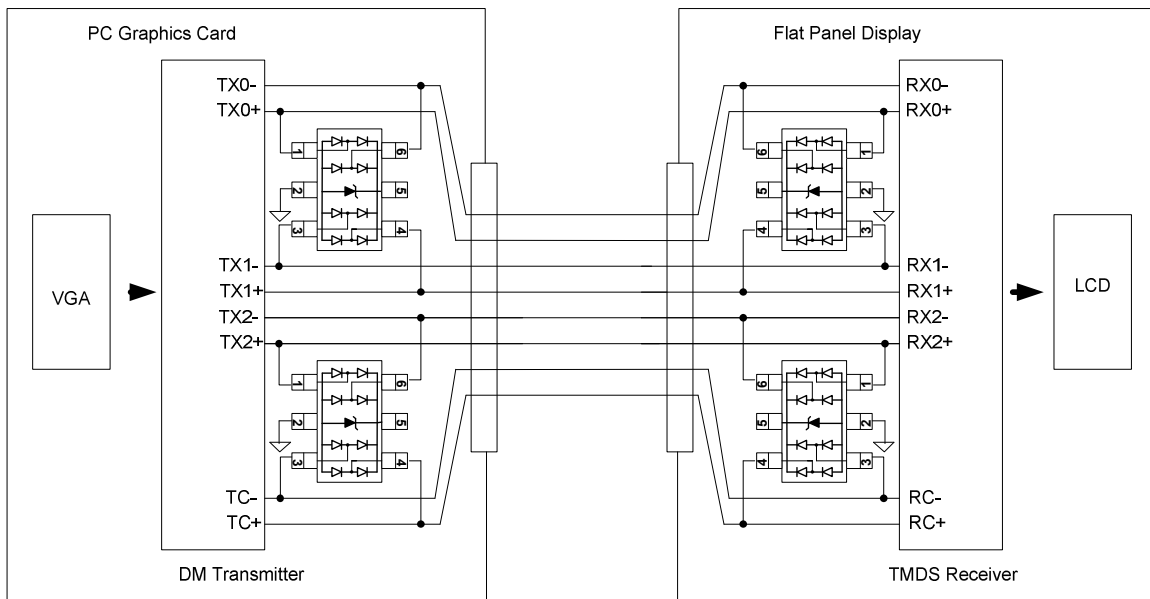
USRV05-4 on USB Port Application



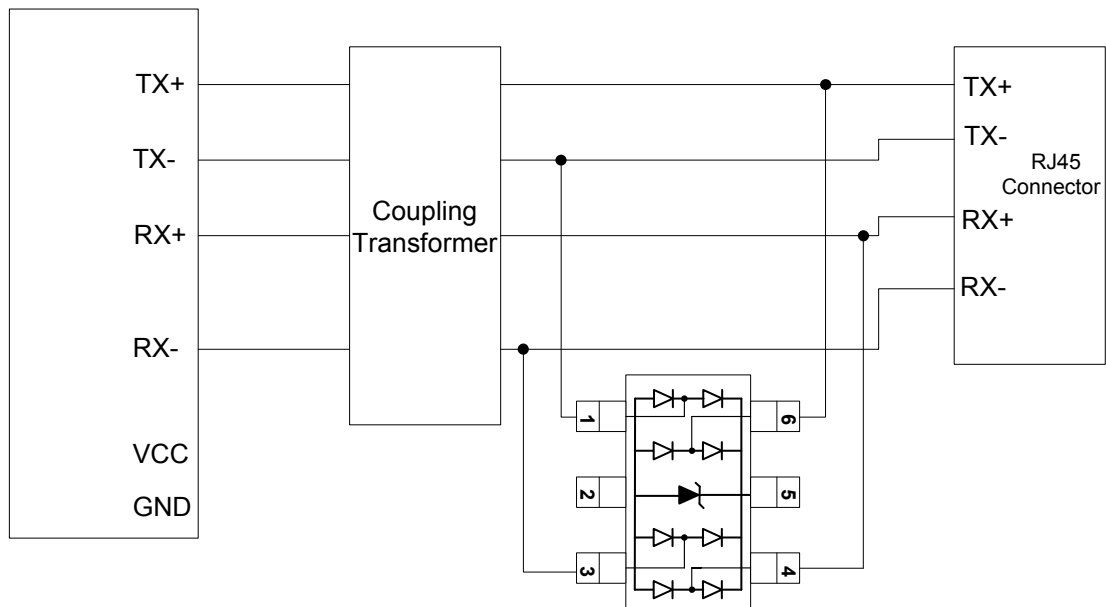
USRV05-4 on SIM Port Application



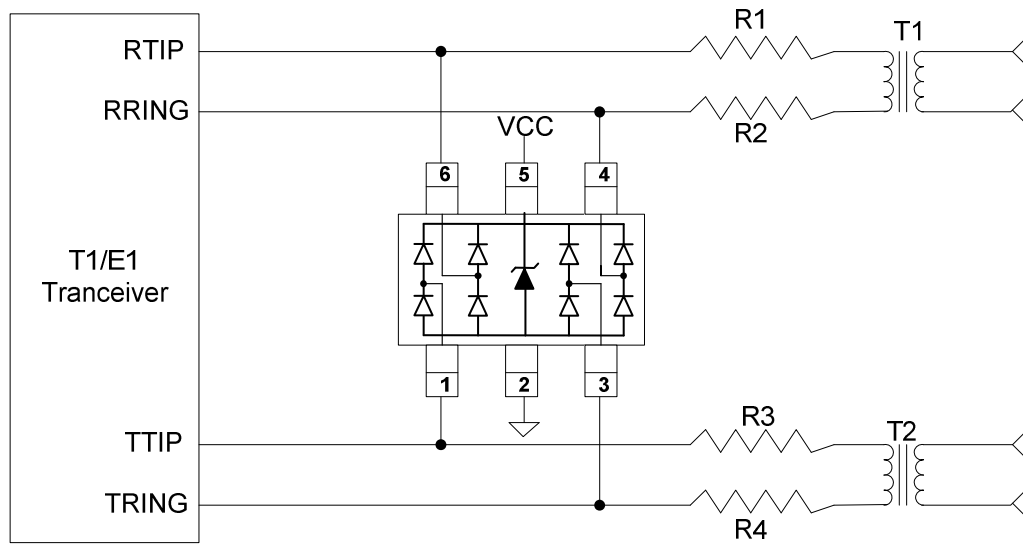
USRV05-4 on Digital Visual Interface(DVI) Application



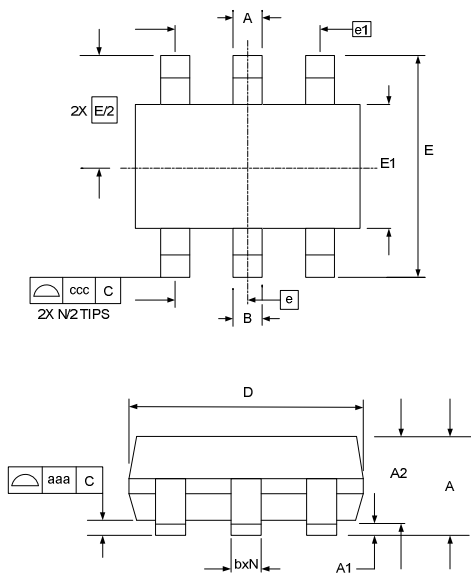
USRV05-4 on Ethernet 10/100(Differential mode) Application



USRV05-4 on T1/E1 Interface Application

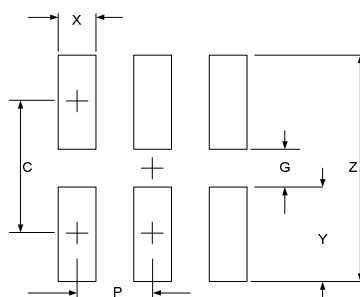


SOT23-6 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90		1.45	0.035		0.057
A1	0.00		0.15	0.000		0.006
A2	0.90	1.15	1.30	0.035	0.045	0.051
b	0.25		0.50	0.010		0.020
c	0.08		0.22	0.003		0.009
D	2.80	2.90	3.10	0.110	0.114	0.122
E1	1.50	1.60	1.75	0.060	0.063	0.069
E	2.80 BSC			0.110 BSC		
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
N	6			6		
aaa	0.10			0.004		
ccc	0.20			0.008		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	2.50	0.098
G	1.40	0.055
P	0.95	0.037
X	0.60	0.024
Y	1.10	0.043
Z	3.60	0.141